IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of:		
	Ma, et al.	
Serial No.:	09/374,502	Art Unit: 2815
Filed:	August 13, 1999	
		Examiner: J. Fenty
For:	ISOLATION STRUCTURE CONFIGURATIONS FOR MODIFYING STRESSES IN SEMICONDUCTOR DEVICES	
Attorney Docket No.:	42390.P6623	

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

APPEAL BRIEF
IN SUPPORT OF APPELLANTS' APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicants (hereafter "Appellants") hereby submit this Brief in triplicate in support of his Appeal from a final decision by the Examiner in the above-captioned case. Appellant respectfully requests consideration of this Appeal by the Board of Patent Appeals and Interferences for allowance of the claims in the above-captioned patent application.

An oral hearing is not desired.

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I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge, there are no appeals or interferences related to the present appeal, which will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1-24 and 31 are the subject of the present appeal. Claims 1, 2, 5, 8, 15, 18, 20, 23, and 31 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,083,797 issued July 4, 2000 to Shyh-Chyi Wong and Shi-Tron Lin (hereinafter "the Wong patent"). Claims 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22, and 24 stand rejected under 35 U.S.C. § 103(a) as being obvious over the Wong patent in view of the U.S. Patent No. 5,395,790 issued March 7, 1995 to Water Lur (hereinafter "the Lur patent").

IV. STATUS OF AMENDMENTS

In response to the Final Office Action mailed on August 27, 2002 and the Advisory Action mailed on November 29, 2002, Appellants timely filed a Notice of Appeal on December 11, 2002. No pending claims have been amended.

A copy of all claims on appeal, claims 1-24 and 31, is attached hereto as Appendix A.

V. SUMMARY OF THE INVENTION

The present invention relates to apparatus and methods for modifying isolation structure configurations, such as trench depth and isolation materials, to modify (i.e., induce or reduce) tensile and/or compressive stresses on an active area of a semiconductor device. In specific, the present invention relates to a semiconductor device having an active area formed in a semiconductor substrate and an isolation structure, substantially surrounding the active area, comprising at least one dielectric material disposed within a trench in the semiconductor substrate, and wherein a portion of the isolation structure is adapted to modify stresses incurred on the active area. Summary of the Invention, page 4, line 24 through page 5, line 2.

It is known that stresses on an active area can significantly affect the performance of MOS (Metal Oxide Semiconductor) devices. For nMOS devices, tensile stress in both directions improves performance, while compressive stress degrades performance. For pMOS devices, tensile stress perpendicular to the channel current direction improves performance, but tensile stress parallel to the channel current direction degrades performance, and vice versa for compressive stress. Background of the Invention, page 3, lines 11-23.

It would be advantageous to modify the stresses acting upon a MOS device active area in order to improve performance. Such stress modification might be achieved at the packaging level by applying stresses to the semiconductor die. However, semiconductor dice are usually brittle and break easily under stress. Additionally, it is very difficult to apply a uniform stress across an entire semiconductor die. Thus, applying a uniform stress across the semiconductor die may result in non-uniform stress that may result in undesirable performance variations in the devices across the semiconductor die. Detailed Description, page 7, lines 7-14.

FIGs. 1 and 2 illustrate an invention embodiment for an nMOS device 100. The nMOS device 100 comprises an n-type source region 102 and an n-type drain region 104, which are implanted into a semiconductor substrate 106 by any known implantation technique. Gate structure 108 spans a region of semiconductor substrate 106 between source region 102 and drain region 104. Generally, gate structure 108 comprises a conductive material 112 electrically isolated with dielectric spacers 114 and 114' adjacent source region 102 and drain region 104, a lower dielectric layer 116, and a cap layer 118. Detailed Description, page 9, line 15-22.

Source region 102 and drain region 104 are isolated with an isolation structure 122 extending into semiconductor substrate 106. Isolation structure 122 surrounds source region 102 and drain region 104, shown in FIG. 2, to form an active area 124. Isolation structure 122 includes a dielectric material 126 that has a lower modulus (i.e., more compliant) than semiconductor substrate 106. Exemplary low-modulus, dielectric materials 126 include, but are not limited to, polymers and porous oxides. As shown in FIG. 3, when compressive stresses (arrows 128) are incurred on the semiconductor die, such as through flip-chip packaging stress, the low-modulus, dielectric material 126 deforms, thereby eliminating or lessening the detrimental effect of compressive stress 128 on active area 124. FIG. 4 shows a stress model, which illustrates this effect. FIG. 4 shows that under 100 MPa compressive stress applied to a semiconductor die front surface, the average stress in the active area (the vertical axis) depends on the modulus of the trench dielectric material. The horizontal axis is active area dimension along the direction of applied stress. Curve A represents a trench filled with a silicon

dioxide with a modulus of between about 70 and 80 GPa. Curve B represents a similar trench filled with a complaint dielectric material, specifically polyimide with a modulus of about 5 GPa. Thus, FIG. 4 illustrates that compressive stress on the active areas can be reduced by using more compliant dielectric materials. This compressive stress reduction is more significant for smaller dimension active areas. Detailed Description, page 7, line 23 through page 8, line 12.

FIGs. 5 and 6 illustrate another embodiment for a pMOS device 130. The pMOS device 130 is similar to nMOS device 100 illustrated in FIGs. 1 and 2 except that pMOS device 130 has a p-type source region 132 and a p-type drain region 134. As previously discussed for pMOS devices, tensile stress perpendicular to channel current direction improves performance, but tensile stress parallel to channel current direction degrades performance, and vice versa for compressive stress. In FIG. 6, to improve performance of the pMOS device, low-modulus, dielectric material 126 is placed in isolation structure 122 parallel to channel current direction to eliminate or lessen detrimental compressive stress perpendicular to channel current direction. Furthermore, a high-modulus (stiff), dielectric material 136 is placed in isolation structure 122 perpendicular to channel current direction to translate beneficial compressive stress parallel (arrows 128) to channel current direction to active area 124. High-modulus, dielectric material 136 should have a modulus equal to or higher than a modulus of semiconductor substrate 106. Therefore, any stresses incurred on high-modulus, dielectric material 136 will also be incurred on active area 124 with substantially the same force (arrows 138). Exemplary high-modulus, dielectric materials 136 include, but are not limited to, silicon nitride and silicon dioxide deposited to have compressive stresses. Detailed Description, page 9, line 1-19.

The use of low-modulus, dielectric material can also improve pMOS device performance in back-bonded packaging configurations. FIGs. 7 and 8 illustrate a back-bonded package 140. With such configurations, a back surface 142 of a semiconductor die 144 is attached to a carrier substrate 146. Electrical communication between semiconductor die 144 and carrier substrate 146 is generally achieved by bond wires 148 extending between electrical traces on or in an active surface of semiconductor die 144 and electrical traces on carrier substrate 146. The attachment of the semiconductor die back surface 142 to carrier substrate 146 achieved with an adhesive material 152, as shown in FIG. 7. The resulting structure is then heated to cure adhesive material 152. However, when the resulting structure is cooled down to room temperature from the adhesive material cure temperature, a bending curvature develops because the carrier substrate 146 contracts more than the semiconductor die 144 (i.e., due to the thermal expansion mismatch between the carrier substrate 146 and the semiconductor die

144), as shown in FIG. 7. Such bending causes biaxial tensile stresses (illustrated by arrows 154 in FIG. 8) on the MOS transistors (shown schematically as rectangles 156 in FIG. 8) within the semiconductor die 144. Detailed Description, page 9, line 20 through page 10, line 6.

Of course, these biaxial tensile stresses enhance performance of nMOS devices, but have little effect on the performance of a pMOS device, due to the cancellation effects of the two perpendicular stress components. However, low-modulus, dielectric material 126 can be used to improve the performance a pMOS device. As shown in FIG. 9, the low-modulus, dielectric material 126 is placed in isolation structure 122 perpendicular to the channel current direction to eliminate or lessen the detrimental tensile stress parallel to the channel current direction of pMOS device 150. The parallel tensile stress is eliminated or lessened, because when parallel tensile stress (arrows 154 in FIG. 9) is incurred on the semiconductor die, the low-modulus, dielectric material 126 stretches, as shown in FIG. 10, thereby eliminating or lessening the detrimental effect of the tensile stress 128 on the active area 124. Furthermore, referring to FIG. 9, a high-modulus (stiff), dielectric material 136 may be placed in isolation structure 122 parallel to channel current direction to translate beneficial tensile stress perpendicular to the channel current direction to active area 124 (translated tensile stress shown as arrows 158). Detailed Description, page 10, line 7 through page 10, line 21.

FIGs. 11 and12 illustrate yet another embodiment for an nMOS device 160. The nMOS device 160 illustrated in FIGs. 11 and 12 is similar to nMOS device 100 illustrated in FIGs. 1 and 2. However, with the present embodiment, isolation structure 122 includes a dielectric material 162 that has tensile stress-inducing properties (e.g., creates tensile stress on adjacent structures and/or materials). Exemplary tensile stress-inducing, dielectric materials 162 include, but are not limited to, silicon nitride that has been deposited to have large tensile stresses. In FIG. 11, the tensile stress-inducing, dielectric material 162 creates a tensile stress (arrows 164) on the active area 124 thereby improving the performance of the nMOS device, even when no external stresses are incurred on the semiconductor die. However, when compressive stresses (arrow 128) are incurred on the semiconductor die, tensile stress-inducing, dielectric material 162 creates the tensile stress (arrows 164) on active area 124 in a direction opposite compressive stresses 128, which eliminates or lessens the detrimental effect of compressive stress 128. Detailed Description, page 10, line 22 through page 11, line 5.

FIG. 13 illustrates still another embodiment for a pMOS device 170. The pMOS device 170 is similar to pMOS device 130 illustrated in FIGs. 5 and 6. As previously discussed for pMOS devices, tensile stress perpendicular to channel current direction improves performance,

but tensile stress parallel to channel current direction degrades performance, and vice versa for compressive stress. To improve the performance of the pMOS device, tensile stress-inducing, dielectric material 162 is placed in isolation structure 122 parallel to channel current direction to eliminate or lessen detrimental compressive stress perpendicular to channel current direction. Thus, a compressive stress-inducing, dielectric material 166 may be placed in isolation structure 122 perpendicular to channel current direction to induce beneficial compressive stress (arrows 168) parallel to the channel current direction to the active area 124. Compressive stress-inducing, dielectric material 166 creates a compressive stress on adjacent structures and/or materials. Compressive stress-inducing, dielectric materials 166 may include, but are not limited to, silicon nitride and silicon dioxide deposited to have compressive stresses. Thus, the configuration shown in FIG. 13 improves the performance of the pMOS device when no external stresses are incurred on the semiconductor die or when biaxial compressive or tensile stresses are incurred on the semiconductor die. Detailed Description, page 11, line 6-24.

A further embodiment increases isolation structure depth to reduce compressive stresses. FIGs. 14 and 15 illustrate a model structure and a graph of the results of a numerical simulation using the finite element method for the model structure. In FIG. 14, A is active area width (or length), B is isolation structure width, H is trench depth and D is active area depth. In the simulation, trench width B was fixed at 0.5 microns (stress incurred on the active area is not significantly sensitive to trench width) and active region depth D is fixed at 0.25 um. Thus, active area width A and isolation structure depth H are variables. FIG. 15 illustrates simulation results with a dielectric material having a modulus of about 5 GPa, where the horizontal axis is trench depth H, and the vertical axis is compressive stress in active area normalized by semiconductor die/packaging thermal mismatch stress. The simulation was performed for three active area widths (i.e., A=2.0um corresponding to curve A1, A=1.0um corresponding to curve A2, and A=0.5um corresponding to curve A3) covering a range of interest. As FIG. 15 illustrates for all the three active area widths, compressive stresses decreased and approached zero with an increase of trench depth. Furthermore, it is observed that the smaller the active area width A, the less the active area is affected by applied stress. Increased trench depth makes carrier substrate 106 more flexible. Thus, when a dielectric material which is more compliant than the carrier substrate is used, stress on the active area is decreased. Preferably, the structure should have a trench depth H to active area width A aspect ratio (i.e., H/A) of greater than about 0.5. Detailed Description, page 11, line 25 through page 12, line 15.

FIGs. 16 and 17 illustrates the deep trench embodiment of the present invention for an nMOS device 172. The nMOS device 172 illustrated in FIG. 16 is similar in structure to the nMOS device 100 illustrated in FIGs. 1. However, with the present embodiment, the isolation structure depth is increased to form deep isolation structure 174. The increased depth of the deep isolation structure 174 has been found to reduce compressive stresses on the active area 124. FIG. 17 illustrates a configuration wherein the deep isolation structure 174 surrounds the active area 124. The deep isolation structure 174 includes a dielectric material 178 disposed therein. With the deep isolation structure 174, a standard dielectric material 178, such as silicon dioxide, may be used to isolate the active area 124. However, to further enhance the reduction in compressive stress, the dielectric material 178 may be a low-modulus dielectric material (described in FIGs. 1 and 2) or a tensile stress-inducing, dielectric material (described in FIGs. 11 and 12). Detailed Description, page 12, line 16 through page 12, line 28.

FIG. 18 illustrates the deep trench embodiment of the present invention for a pMOS device 180 with the deep trenches formed perpendicular to the channel current direction. The pMOS device 180 illustrated in FIG. 18 is similar to the nMOS device 130 illustrated in FIG. 5. Detailed Description, page 12, line 29 through page 13, line 2.

In FIG. 19, when pMOS device 180 is subjected to biaxial compressive stresses, isolation structure depth is increased only in portions 182 of isolation structure 122 that are parallel to channel current direction to eliminate or lessen detrimental compressive stresses perpendicular to the channel current direction. To further reduce detrimental compressive stresses on active area 124 perpendicular to channel current direction, a low-modulus dielectric material (described in FIG. 6) or a tensile stress-inducing, dielectric material (described in FIG. 13) may be disposed in isolation structure portions 182. Portions 184 of isolation structure 122 that are perpendicular to the channel current direction are of a depth sufficient to isolate active area 124, but may translate beneficial compressive stress to active area 124 parallel to the channel current direction. In order to further translate or induce beneficial compressive stress to active area 124 parallel to the channel current direction, a high-modulus dielectric material (described in FIG. 6) or a compressive stress-inducing, dielectric material (described in FIG. 13) may be disposed in isolation structure portions 184. Detailed Description, page 13, line 3-19.

When pMOS device 190 is subjected to biaxial tensile stresses, isolation structure depth is increased only in portions 192 of isolation structure 122 that are perpendicular to channel current direction in order to eliminate or lessen detrimental tensile stresses parallel to the channel current direction, as shown in FIG. 20. In order to further reduce detrimental tensile

stresses on the active area 124 perpendicular to the channel current direction, a low-modulus dielectric material (described in FIG. 6) or a compressive stress-inducing, dielectric material (described in FIG. 13) may be disposed in isolation structure portions 192. Portions 194 of isolation structure 122 which are parallel to the channel current direction are of a depth sufficient to isolate active area 124, but may translate beneficial tensile stress to active area 124 perpendicular to the channel current direction. In order to further translate or induce beneficial tensile stress to active area 124 perpendicular to the channel current direction, a high-modulus dielectric material (described in FIG. 9) or a tensile stress-inducing, dielectric material (described in FIG. 13) may be disposed in isolation structure portions 194. Detailed Description, page 13, line 20 through page 14, line 5.

The introduction of various low-modulus and high-modulus dielectric material, and compressive stress-inducing and tensile stress-inducing dielectric materials may degrade the interface between the active area and the dielectric material and cause leakage problems. Thus, a thin conformal barrier layer 196, such as silicon dioxide 196, may be deposited in isolation structure 122 prior to depositing any of dielectric materials 198, as shown FIG. 21. Detailed Description, page 14, line 6 through page 14, line 11.

VI. ISSUES PRESENTED

Whether claims 1, 2, 5, 8, 15, 18, 20, 23, and 31 are anticipated under 35 U.S.C. § 102(e) over the Wong patent.

Whether claims 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22, and 24 are obvious over 35 U.S.C. § 103(a) over the Wong patent in view of the Lur patent.

VII. GROUPING OF CLAIMS

For the purposes of this appeal:

Claims 1, 2, 5, 8, 15, 18, 20, 23, and 31 stand or fall together as Group I;

Claims 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22, and 24 stand or fall together as Group II;

Reasons for separate patentability of the above-indicated Claim Groups I and II are presented in the argument section pursuant to 37 C.F.R. §1.192(c)(5).

VIII. ARGUMENT

A. REJECTION OF CLAIMS 1, 2, 5, 8, 15, 18, 20, 23, AND 31 UNDER 35 U.S.C. § 102(e) OVER THE WONG PATENT IS IMPROPER. THE WONG PATENT DOES NOT TEACH OR SUGGEST ALL OF THE CLAIM LIMITATIONS OF CLAIMS 1, 2, 5, 8, 15, 18, 20, 23, AND 31, NOR DOES IT SHOW THE IDENTICAL INVENTION IN AS COMPLETE DETAIL AS IS CONTAINED IN THE CLAIMS

The Examiner has rejected claims 1, 2, 5, 8, 15, 18, 20, 23, and 31 under 35 U.S.C. § 102(b) as being unpatentable over the Wong patent.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The first independent claim of Claim Group I, claim 1, is drawn to a semiconductor device, comprising an active area formed in a semiconductor substrate, and an isolation structure comprising at least one dielectric material disposed within a trench which extends into the semiconductor substrate, wherein the isolation structure substantially surrounds the active area, and wherein at least a portion of the isolation structure is adapted to modify stresses incurred on the active area. Claim 2 depends from claim 1 and includes the additional limitation of the active area further comprises nMOS device components including an n-type source region, an n-type drain region, and a gate structure disposed adjacent the active area between the n-type source region and the n-type drain region. Claim 5 depends from claim 2 and includes the additional limitation that the active area includes a width and wherein the isolation structure comprises at least a portion of the trench having a depth such that an aspect ratio of the trench portion depth to the active area width is greater than about 0.5. Claim 8 depends from claim 1 and includes the additional limitation that the active area further comprises pMOS device components including a p-type source region, a p-type drain region, and a gate structure disposed adjacent the active area between the p-type source region and the p-type drain region. Claim 15 depends from claim 1 and includes the additional limitation that the isolation structure comprises at least a portion of the trench parallel to a channel current direction of the pMOS device components having a depth wherein the active area includes a width and wherein the

isolation structure comprises at least a portion of the trench parallel to a channel current direction of the pMOS device having a depth such that an aspect ratio of the trench portion depth to the active area width is greater than about 0.5. Claim 18 depends from claim 15 and includes the additional limitation that the isolation structure comprises a high-modulus, dielectric material disposed within at least a portion of the trench perpendicular to the channel current direction of the pMOS device components. Claim 20 depends from claim 8 and includes the additional limitation that the active area includes a width and wherein the isolation structure comprises at least a portion of the trench perpendicular to a channel current direction of the pMOS device components having a depth such that an aspect ratio of the trench portion depth to the active area width is greater than about 0.5. Claim 23 depends from claim 1 and includes the additional limitation that the isolation structure comprises a high-modulus, dielectric material disposed within at least a portion of the trench parallel to the channel current direction of the pMOS device components.

The second independent claim of Claim Group I, claim 31, is drawn to a semiconductor device, comprising an active area formed in a semiconductor substrate, and a stress modifying isolation structure comprising at least one dielectric material disposed within a trench which extends into the semiconductor substrate, wherein the isolation structure substantially surrounds the active area.

The Appellants respectfully assert that the Wong patent is inapplicable with regard to a Section 102(e) rejection. The Appellants have repeatedly pointed out that the Office has not shown that the Wong patent teaches or suggests each and every limitation of the claims. In particular, there is no teaching of a portion of the isolation structure being adapted to modify stresses incurred on the active area.

In the January 17, 2002 Response and the October 28, 2002 Response After Final Rejection, the Appellants pointed out that:

> In the "Response to Arguments" on page 6, the Office Action, by its own admissions, has rendered the present rejection moot. The Office Action states that "It can be interpreted that though the isolation dielectrics of Wong are considered, 'high modulus,' they still will have an effect on the stresses of the silicon substrate, which is what the claims imply." With the words of "It can be interpreted", the Section 102(e) rejection fails, because the Office Action has to add something beyond the teaching of the Wong patent. Further, the Office Action states that the isolation dielectrics "will have an effect on the stresses of the silicon substrate". This is a mere conjecture, as there is no such teaching within the Wong patent. Thus, in order to make the Wong patent "fit", the Official Action has to add to the teaching of the Wong patent with its own interpretations and conjectures. The moment that this occurs, the Section 102(e) rejection fails,

because "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference", not in the interpretations and conjectures of the Office.

In response to the Appellants arguments, the August 27, 2002 Final Office Action at page 6 ("Response to Arguments") states the "[t]he STI region (12) of Wong is *inherently* 'adapted to modify stresses incurred in the active area,' by the mere placement of the regions in the active area."

In the October 28, 2002 Response After Final Rejection, the Appellants pointed out that the Office's inherency contention is insufficient. As set forth in M.P.E.P. § 2112:

> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of the result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstance is not sufficient.'" In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

Unfortunately, the Office has not presented any extrinsic evidence, basis in fact, and/or technical reasoning to support its inherency contention. Therefore, the Office's inherency contention is without merit.

In response to this, the November 29, 2002 Advisory Action contends:

> . . . regarding inherency, if the teachings of the prior art anticipate the disclosure of the claimed invention, then the structure of the prior art will function in the same manner as the claimed invention. Such will be recognized by one of ordinary skill in the art. Such correlation is not a "probability or a possibility." Rather the correlation is a one-to-one matching of elements in the claim against the prior art.

However, that it is the point, the Office has not shown a one-to-one matching of elements in the claim against the prior art, as it has failed to show the limitation of a portion of the isolation structure being adapted to modify stresses incurred on the active area or that it is an inherent characteristic of the prior art.

To compensate for the lack of teaching, the November 29, 2002 Advisory Action continues with:

> . . . the isolation structure of the prior art, based on a similar inherency argument, will necessarily be "stress-modifying." One skilled in the art will recognize that an isolation structure of a different material than that of the substrate will modify the rigidity of the structure, either making the substrate more of less rigid, but "modifying the stress" nonetheless.

The November 29, 2002 Advisory Action's contention is shockingly inaccurate. The fact that an isolation structure is of a different material than that of the substrate does not mean that it will modify stresses incurred in the active area. As the Office should certainly know, isolation structures can be "stress-free", neither imparting a tensile or compressive stress on the active area, as stress-free isolation structures are discussed in the Lur patent, which the Office relied upon for the Section 103(a) rejection of claims in the present application. For example, the present application discusses silicon nitride as being capable of being either tensile or compress inducing depending on the deposition technique. As the Office should well know that silicon nitride can be deposited to be "stress-free" (i.e., in between tensile and compressive). Thus, it is clear that the November 29, 2002 Advisory Action's contention is without merit.

Furthermore, with regard to independent claim 1 and independent claim 31, the August 27, 2002 Final Office Action at page 2 and at page 4, respectively, contends that the Wong patent teaches that the "isolation structure substantially surrounds said active area". The January 17, 2002 Response and the October 28, 2002 Response After Final Rejection pointed out that the September 17, 2001 Office Action and the August 27, 2002 Final Office Action, respectively, did not show any teaching in the Wong patent that the isolation structure substantially surrounds the active area. The Final Office Action responded at page 6 stating that "looking at Figure 2D, one skilled in the art will see that the STI region (12) is placed on either side of the active region, as well as in between the N and P channel transistors, thus, surrounding each active region." This contention is respectfully believed to be inaccurate. At best, the Figure 2D shows is that the STI regions (12) potentially extending a direction perpendicular to the plane of the drawing, not that the STI regions "substantially surround" the active region as defined in the present application (see FIG. 2 of the current application). Thus, as "each and every element" of the claims is not taught by the Wong patent, the rejection to independent claim 1 (and its dependent claims 2, 5, 8, 15, 20, and 23) and independent claim 31 is without merit.

The August 27, 2002 Final Office Action at page 2 further contends that the limitation in independent claim 1 (from which claim 3, 5, 8, 15, 18, 20, and 23 either directly or indirectly depend) of "wherein at least a portion of said isolation structure is adapted to modify stresses

incurred on said active area" is a recitation of the intended use of the claimed invention and does not differentiate the claimed composition of the elements from those known to prior art. Appellants respectfully disagree with this assessment and believe the limitation to be valid. Although M.P.E.P. § 2106 gives "adapted to" as one example of language that may raise a question as to the limiting effect, the Section also sets forth that "[t]he subject matter of a properly construed claim is defined by the terms that limit its scope. It is this subject matter that must be examined. As a general matter, the grammar and intended meaning of terms used in a claim will dictate whether the language limits to claim scope. Language that suggests or makes optional but does not require step to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation." The limitation of "adapted to modify stresses incurred on said active area" in claim 1 is not optional. If the isolation structure is not structurally adapted to modify stresses incurred on the active area, then it does not fall within the scope of the present claims. Therefore, the limitation is valid and the Wong patent neither teaches nor suggests an isolation structure that modifies stresses incurred on the active area.

Appellants added independent claim 31 in an Amendment filed June 19, 2001, which claims in total: "A semiconductor device, comprising: an active area formed in a semiconductor substrate; and a stress modifying isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area." Although the claim does not use "adapted to" language, the Office contended that the rejection of "intended use" still applies. However, the limitation of a "stress modifying" isolation structure is no different than a limitation of "metal" in a claim stating "a metal rod". If a rod shown in a prior art reference is not metal then it cannot be used as in a Section 102 rejection, because the prior art reference must be in "as complete detail as is contained in the claim". Likewise, the Wong patent does not teach or suggest a "stress modifying" isolation structure, and, thus, it fails as a Section 102(e) rejection.

With regard to claims 5, 15, and 20, the August 27, 2002 Final Office Action contends that the Wong patent teaches a trench has a depth in ratio to the active area width is greater than 0.5. However, as pointed out in the January 17, 2002 Response, the Final Office Action does not specifically show any teaching in the Wong patent of such a ratio, nor could the Appellants find any such teaching. Moreover, not even the drawings show such a ratio between the STI depth and the width of the active area. Surprisingly, the August 27, 2002 Final Office Action at page 7 admits this and states that "one skilled in the art, through routine

experimentation would have been able to compute an aspect ratio in the range claimed in the present invention." With that admission, the Section 102 rejection fails. The Appellants respectfully find it odd that the Final Office Action does not seem to comprehend the difference between a Section 102 and Section 103 rejection in this regard. Nonetheless, as this limitation is neither taught nor suggested by the Wong patent, the Section 102(e) rejection to these claims is improper.

Furthermore, the November 29, 2002 Advisory contains the odd statement "though the prior may not explicitly claim an "aspect ratio" of 0.5, dimensions are given in the prior art, that when inserted into the formula provided by the applicant, the height/area as disclosed satisfies the value of "greater than about 0.5". Yet again, the Office admits that the Section 102(e) rejection is not valid and, oddly, uses the Appellants' teaching to achieve an improper hindsight reconstruction.

Thus, it is clear that by the Office Action's own admission and from the actual teachings of Wong patent that the Section 102(e) is without merit. Therefore, as the Wong patent neither teaches nor suggests "each and every element" of claims 1, 2, 5, 8, 15, 20, 23, and 31, and further as the Office has not shown that the Wong patent illustrates the "identical invention . . . in as complete detail as is contained in the claim" with regard to the claims, Appellants submit that claims 1, 2, 5, 8, 15, 18, 20, 23, and 31 recite patentable subject matter.

B. REJECTION OF CLAIMS 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22, and 24 UNDER 35 U.S.C. § 103(a) OVER THE WONG PATENT IN VIEW OF THE LUR PATENT IS IMPROPER, AS THE OFFICE DID NOT MEET ALL OF THE LIMITATIONS IN ALL OF THE CLAIMS, AND, THUS, DID NOT ESTABLISH A PRIMA FACIE CASE OF OBVIOUSNESS

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The Examiner has rejected claims 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22, and 24 under 35 U.S.C. § 103(a) as being obvious over the Wong patent in view of the Lur patent.

Claim 3 depends from claim 2 and includes the additional limitation that the isolation structure comprises a low-modulus, dielectric material disposed within at least a portion of the trench. Claim 4 depends from claim 2 and includes the additional limitation that the isolation structure comprises a tensile stress-inducing, dielectric material disposed within at least a portion of the trench. Claim 6 depends from claim 5 and includes the additional limitation that the the isolation structure comprises a low-modulus, dielectric material disposed within at least a portion of the trench. Claim 7 depends from claim 5 and includes the additional limitation that the isolation structure comprises a tensile stress-inducing, dielectric material disposed within at least a portion of the trench. Claim 9 depends from claim 8 and includes the additional limitation that the isolation structure comprises a low-modulus, dielectric material disposed within at least a portion of the trench parallel to a channel current direction of the pMOS device components. Claim 10 depends from claim 9 and includes the additional limitation that the isolation structure comprises a high-modulus, dielectric material disposed within at least a portion of the trench perpendicular to the channel current direction of the pMOS device components. Claim 11 depends from claim 8 and includes the additional limitation that the isolation structure comprises a low-modulus, dielectric material disposed within at least a portion of the trench perpendicular to a channel current direction of the pMOS device components. Claim 12 depends from claim 11 and includes the additional limitation that the isolation structure comprises a high-modulus, dielectric material disposed within at least a portion of the trench parallel to the channel current direction of the pMOS device components. Claim 13 depends from claim 8 and includes the additional limitation that the isolation structure comprises a tensile stress-inducing, dielectric material disposed within at least a portion of the trench parallel to the channel current direction of the pMOS device components. Claim 14 depends from claim 8 and includes the additional limitation that the isolation structure comprises a compressive stress-inducing, dielectric material disposed within at least a portion of the trench perpendicular to the channel current direction of the pMOS device components. Claim 16 depends from claim 15 and includes the additional limitation that the isolation structure comprises a low-modulus, dielectric material disposed within at least a portion of the trench parallel to the channel current direction. Claim 17 depends from claim 15 and includes the additional limitation that the isolation structure comprises a tensile stress-inducing, dielectric material disposed within at least a portion of the trench parallel to the channel current direction. Claim 19 depends from claim 15 and includes

the additional limitation that the isolation structure comprises a compressive stress-inducing, dielectric material disposed within at least a portion of the trench perpendicular to the channel current direction of the pMOS device components. Claim 21 depends from claim 20 and includes the additional limitation that the isolation structure comprises a low-modulus, dielectric material disposed within at least a portion of the trench perpendicular to the channel current direction of the pMOS device components. Claim 22 depends from claim 20 and includes the additional limitation that the isolation structure comprises a compressive stress-inducing, dielectric material disposed within at least a portion of the trench perpendicular to the channel current direction of the pMOS device components. Claim 24 depends from claim 20 and includes the additional limitation that the the isolation structure comprises a tensile stress-inducing, dielectric material disposed within at least a portion of the trench parallel to the channel current direction of the pMOS device components.

Claims 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22, and 24 depends either directly or indirectly from claim 1. Thus, all of the limitations of claim 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22, and 24 are rejected over the Wong patent in an identical manner as the Section 102(e) rejection. Therefore, all of the responses with regard to the Section 102(e) rejection of claims1, 2, 5, 8, 15, 18, 20, 23 are equally applicable to the present rejection of claims 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22, and 24 and are hereby incorporated herein by reference as though repeated in total.

As previously discussed for the Section 102(e) rejection, the Wong patent does not teach or suggest that the isolation structure modifies stresses, nor does the Wong patent teach that the isolation structure substantially surrounds the active area, as required for independent claim 1 (from which claims 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22, and 24 either directly or indirectly depend). The Lur patent is relied upon by the Office Action for a teaching of a low-modulus dielectric material. Thus, the Lur patent does not overcome the deficiencies in the teaching of the Wong patent. Therefore, even if the Wong patent and the Lur patent were properly combined that presently claimed invention would not be taught or suggested.

More specifically, the Office Action relies upon a teaching of a polyimide used as an insulating material in the Lur patent as a teaching of a low-modulus material. However, the term "polyimide" covers a range of polymer compounds that may or may not be low-modulus. Thus, there is no direct teaching of the requirement of the "polyimide" to be low-modulus.

Furthermore, the Lur patent does not overcome the lack of teaching or suggestion within the Wong patent for an isolation structure that modifies stresses. If fact, it is quite the opposite, as the Lur patent teaches that the isolation structure should be "stress-free" (col. 5, line 20).

Moreover, the Lur patent does not overcome the lack of teaching or suggestion within the Wong patent for an isolation structure that substantially surrounds an active area. The Lur patent merely teaches a method of forming an isolation structure.

Additionally, the Office Action at pages 5 and 6 makes the statement that "[t]he dielectric material is disposed in the trench both parallel and perpendicular to the channel current direction". The Appellants could not find any such teaching or suggestion in either the Wong patent or the Lur patent. The Appellants respectfully request that the Office disclose the location of such a teaching.

It is clear from the deficiencies in the teaching of the Wong patent and the insufficient teaching in the Lur patent to overcome these deficiencies that the combination of these references do not teach or suggest all of the claim limitations of claims 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22, and 24. Thus, as the Office has not shown any teaching or suggestion of all of the limitations of the claims and, therefor, has not established a prima facie case of obviousness, Appellants submit that claims 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22, and 24 recites patentable subject matter.

IX. CONCLUSION

Appellants respectfully submit that all the pending claims in this patent application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted in triplicate, along with a check for $320.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c).

Respectfully submitted,

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APPENDIX A: CLAIMS ON APPEAL

1. A semiconductor device, comprising:

an active area formed in a semiconductor substrate; and

an isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area, and wherein at least a portion of said isolation structure is adapted to modify stresses incurred on said active area.

2. The semiconductor device of claim 1, wherein said active area further comprises nMOS device components including an n-type source region, an n-type drain region, and a gate structure disposed adjacent said active area between said n-type source region and said n-type drain region.

3. The semiconductor device of claim 2, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench.

4. The semiconductor device of claim 2, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench.

5. The semiconductor device of claim 2, wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

6. The semiconductor device of claim 5, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench.

7. The semiconductor device of claim 5, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench.

8. The semiconductor device of claim 1, wherein said active area further comprises pMOS device components including a p-type source region, a p-type drain region, and a gate

structure disposed adjacent said active area between said p-type source region and said p-type drain region.

9. The semiconductor device of claim 8, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench parallel to a channel current direction of the pMOS device components.

10. The semiconductor device of claim 9, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

11. The semiconductor device of claim 8, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to a channel current direction of the pMOS device components.

12. The semiconductor device of claim 11, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

13. The semiconductor device of claim 8, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

14. The semiconductor device of claim 8, wherein said isolation structure comprises a compressive stress-inducing, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

15. The semiconductor device of claim 8, wherein said isolation structure comprises at least a portion of said trench parallel to a channel current direction of the pMOS device components having a depth wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench parallel to a channel current direction of the pMOS device having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

16. The semiconductor device of claim 15, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction.

17. The semiconductor device of claim 15, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction.

18. The semiconductor device of claim 15, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

19. The semiconductor device of claim 15, wherein said isolation structure comprises a compressive stress-inducing, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

20. The semiconductor device of claim 8, wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench perpendicular to a channel current direction of the pMOS device components having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

21. The semiconductor device of claim 20, wherein said isolation structure comprises a low-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

22. The semiconductor device of claim 20, wherein said isolation structure comprises a compressive stress-inducing, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the pMOS device components.

23. The semiconductor device of claim 20, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

24. The semiconductor device of claim 20, wherein said isolation structure comprises a tensile stress-inducing, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the pMOS device components.

31. A semiconductor device, comprising:

an active area formed in a semiconductor substrate; and

a stress modifying isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area.